## $\square$ MN101E16K, MN101E16M

| Type |
| :--- |
| ROM ( $\times 8$-bit) |
| External memory can be expanded |
| RAM ( $\times 8$-bit) |

RAM ( $\times 8$-bit)
External memory can be expanded

| MN101E16K (under planning) | MN101E16M (under development) |
| :---: | :---: |
| 256 K | 384 K |
| 12 K | 20 K |

Package
QFP100-P-1818B *Lead-free (under development), LQFP100-P-1414 *Lead-free (under planning)
Minimum Instruction
$0.0588 \mu \mathrm{~s}$ (at 2.7 V to $3.6 \mathrm{~V}, 17 \mathrm{MHz}$ at internal $2,4,8$ times oscillation used)
$0.1 \mu \mathrm{~s}$ (at 2.7 V to $3.6 \mathrm{~V}, 20 \mathrm{MHz}$ )
$30.6 \mu \mathrm{~s}$ (at 2.7 V to $3.6 \mathrm{~V}, 32.768 \mathrm{kHz}$ )
-RESET • Watchdog • External 0 • External 1 • External 2 •External 3 • External 4 • External 5 •Timer 0
-Timer 1 •Timer $2 \cdot$ Timer $3 \cdot$ Timer $4 \cdot$ Timer $5 \cdot$ Timer $6 \cdot$ Timer 7 (2 systems) •Timer A, B, C, D, E

- Time base •Serial 0 (2 systems) •Serial 1 (2 systems) •Serial $2 \cdot$ Serial 3 ( 2 systems) •Serial 4 (2 systems)
- Automatic transfer finish (2 systems) • A/D conversion finish • Key interrupts

Timer Counter

Timer counter 0 : 8 -bit $\times 1$ (square-wave/8-bit PWM output, event count, simple pulse width measurement, real time output control)
Clock source .................... 1/2, $1 / 4$ of system clock frequency; $1 / 1,1 / 4,1 / 16,1 / 32,1 / 64$ of OSC oscillation clock frequency; $1 / 1$ of XI oscillation clock frequency; external clock input Interrupt source $\qquad$ coincidence with compare register 0

Timer counter 1:8-bit $\times 1$ (square-wave output, event count, synchronous output event, 16 -bit timer with casscade connection (Timer 0 and connection), serial clocke output)
Clock source ..................... 1/2, 1/8 of system clock frequency $1 / 1,1 / 4,1 / 16,1 / 64,1 / 128$ of OSC oscillation clock frequency; $1 / 1$ of XI oscillation clock frequency; external clock input
Interrupt source . $\qquad$ coincidence with compare register 1

Timer counter 0,1 can be cascade-connected.
Timer counter 2 : 8-bit $\times 1$ (square-wave/ 8 -bit PWM output, event count, synchronous output event, pulse width measurement, real time output control, serial baud rate timer)
Clock source .................... 1/2, 1/4 of system clock frequency; $1 / 1,1 / 4,1 / 16,1 / 32,1 / 64$ of OSC oscillation clock frequency; $1 / 1$ of XI oscillation clock frequency; external clock input
Interrupt source $\qquad$ coincidence with compare register 2

Timer counter $0,1,2$ can be cascade-connected.
Timer counter 3:8-bit $\times 1$ (square-wave output, event count, serial baud rate timer)
Clock source .................... $1 / 2,1 / 8$ of system clock frequency; $1 / 1,1 / 4,1 / 16,1 / 64,1 / 128$ of OSC oscillation clock frequency; $1 / 1$ of XI oscillation clock frequency; external clock input
Interrupt source ................. coincidence with compare register 3
Timer counter 2, 3 can be cascade-connected.
Timer counter 0, 1, 2, 3 can be cascade-connected.
Timer counter 6:8-bit freerun timer, time base timer

(square-wave/16-bit PWM output, cycle / duty continuous variable, event count, synchronous output evevt, pulse width measurement, input capture)

> Clock source $\cdots . . . . . . . . . . . . . . . . . . ~$ $\quad 1 / 1,1 / 2,1 / 4,1 / 16$ of system clock frequency; $1 / 1,1 / 2,1 / 4,1 / 16$ of OSC  oscillation clock frequency; $1 / 1,1 / 2,1 / 4,1 / 16$ of external clock input frequency Interrupt source $\cdots . . . . . . . . . . . . . ~ c o i n c i d e n c e ~ w i t h ~ c o m p a r e ~ r e g i s t e r ~$ $7(2$ lines $)$

Timer counter A, B, C, D, E : 8-bit $\times 5$
Clock source .................... 1/2, 1/4 of system clock frequency; $1 / 1,1 / 2,1 / 4,1 / 8,1 / 16.1 / 32$ of OSC oscillation clock frequency
Interrupt source ................ coincidence with compare register A, B, C, D, E
Time base timer (one-minute count setting)
Clock source .................... 1/1 of OSC oscillation clock frequency; 1/1 of XI oscillation clock frequency
Interrupt source $\cdots \cdots \cdots \cdots . . . . . . . .1 / 128,1 / 256,1 / 512,1 / 1024,1 / 8192,1 / 32768$ of clock source frequency
Watchdog timer
Interrupt source $\cdots \cdots . . . . . . . . . . . .1 / 65536,1 / 262144,1 / 1048576,1 / 4194304$ of system clock frequency

| DMA Controller <br> (Automatic Data Transfer) | Nomber of channels : 2 <br> Max. Transfer cycles : 255 <br> Starting factor : external request, various types of interrupt, software <br> Transfer mode : 1-byte transfer, word transfer, burst transfer |
| :---: | :---: |
| Serial Interface | Serial 0 : synchronous type/UART (full-duplex) $\times 1$ <br> Clock source $\qquad$ $1 / 2,1 / 4$ of system clock frequency; pulse output of timer counter $2, A$; 1/2, 1/4, 1/16, 1/64 of OSC oscillation clock frequency |
|  | Serial 1 : synchronous type/UART (full-duplex) $\times 1$ <br> Clock source $\qquad$ $1 / 2,1 / 4$ of system clock frequency; pulse output of timer counter $3, \mathrm{~B}$; $1 / 2,1 / 4,1 / 8,1 / 16,1 / 64$ of OSC oscillation clock frequency |
|  | Serial 2 : synchronous type/single-master $I^{2} \mathrm{C} \times 1$ <br> Clock source $\qquad$ $1 / 2,1 / 4$ of system clock frequency; pulse output of timer counter $3, \mathrm{C}$; $1 / 2,1 / 4,1 / 16,1 / 32$ of OSC oscillation clock frequency |
|  | Serial 3 : synchronous type/ $\mathrm{I}^{2} \mathrm{C} \times 1$ <br> Clock source $\qquad$ $1 / 2,1 / 4$ of system clock frequency; pulse output of timer counter $2, \mathrm{D}$; $1 / 2,1 / 4,1 / 16,1 / 32$ of OSC oscillation clock frequency |
|  | Serial 4 : synchronous type/UART (full-duplex) $\times 1$ <br> Clock source $\qquad$ $1 / 2,1 / 4$ of system clock frequency; pulse output of timer counter $2, \mathrm{E}$; $1 / 2,1 / 4,1 / 16,1 / 64$ of OSC oscillation clock frequency |
| I/O Pins $\quad 1 / 0$ | 22 •(5 V IF port) Common use • Specified pull-up resistor available • Input/output selectable (bit unit) |
|  | 62 •(3 V IF port) Common use • Specified pull-up resistor available • Input/output selectable (bit unit) |
|  | •(3 V IF port) Common use |
| A/D Inputs | 10-bit $\times 8$-ch. (with S/H) |
| Special Ports | Buzzer output, high-current drive port |
| Electrical Characteristics <br> Supply current | T.B.D |
|  |  |

ROM Correction Correcting address designation: up to 7 addresses possible

See the next page for electrical characteristics, pin assignment and support tool.

## Pin Assignment


( ): Flash memory built-in type

## Support Tool

| In-circuit Emulator | Under development |  |
| :---: | :---: | :---: |
| Flash Memory Built-in Type | Type | MN101EF16N (under development) |
|  | ROM ( $\times 8$-bit) | 512 K |
|  | RAM ( $\times 8$-bit) | 30 K |
|  | Minimum instruction execution time | $0.0588 \mu \mathrm{~s}$ (at 2.7 V to $3.6 \mathrm{~V}, 17 \mathrm{MHz}$ ) |
|  | Package | QFP100-P-1818B ${ }^{\text {* Leadfree, }}$ LQFP100-P-1414*Leadffree (under planning) |

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